ABSTRACT

An application specific integrated circuit (ASIC) is disclosed. The ASIC includes a standard cell. The standard cell includes a plurality of logic functions and at least one bus coupled to at least a portion of the logic functions. The standard cell also includes a plurality of internal signals from the plurality of logic functions and a field programmable gate array (FPGA) function coupled to the at least one bus and at least a portion of the plurality of internal signals. The FPGA function includes a debug client function that observes and manipulates the at least one bus and the plurality of internal signals. A system and method in accordance with the present invention utilizes a debug function within a standard cell design to create an internal-to-the-ASIC debugging (software, hardware or both) function. The system and method is provided by connection of internal buses and signals of interest to a debug client function within the FPGA function. The debug client function observes and, if needed, manipulates internal buses and signals and communicates with an external to the ASIC debugging system.